

UfiSpace S9501 Series

Disaggregated Cell Site Gateway Router Specification

Revision 1.0

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2 Revision History

Date	Rev	Author	Summary of Change
Jun. 04, 2021	R1.0	Hector Zhang	First Draft Release

3 Overview

By providing 1GE, 2.5GE, 10GE high speed Ethernet ports and IEEE 1588v2, SyncE timing synchronization features, S9501 Series cell site gateway routers enables service providers to migrate 2G, 3G, 4G BBUs to 5G RAN to firm NSA network, it's also suitable for 5G SA RAN network connection when only 1G/10G ports are necessary.

With temperature-hardened, high port density, high-throughput, small form factor, low-power-consumption & redundancy (PSU and FAN) features, S9501 Series delivers high timing synchronization precision, ultra-low latency, temperature harden and high system reliability, excellent Ethernet switching performance and intelligence to the mobile/radio access network edge in a compact 1RU form factor that helps reduce infrastructure and administrative costs.

S9501 Series SKUs, I/O ports, PSU and FAN configurations are shown as below:

SKU	1G/2.5G/10G Ethernet Ports	FAN	PSU	Timing
S9501-28SMT	4-port 100M/GE RJ45 16-port 100M/GE/2.5G SFP 6-port GE/2.5G/10GE SFP+ 2-port GE/10GE SFP+ w/ MACSec	2+1 Redundant fan FRU	1+1 Redundant 200W PSU FRU AC or DC options	GNSS, ToD, 1PPS, 10M In or Out, T1/E1 Input
S9501-18SMT	4-port 100M/GE RJ45 8-port 100M/GE/2.5G SFP 6-port GE/2.5G/10GE SFP+	2+1 Redundant fab FRU	1+1 Redundant 200W PSU FRU AC or DC options	GNSS, ToD, 1PPS, 10M In or Out

Table 3-1 S9501 Series Configuration Information

The S9501 Series SKUs front panel and rear panel design are shown as below:



Figure 3-1 DCSG Lite ID Rendering -- S9501-28SMT Front Panel



Figure 3-2 DCSG Lite ID Rendering -- S9501-18SMT Front Panel



Figure 3-3 DCSG Lite ID Rendering – Rear Panel (Same for all SKUs)

4 High-Level Description

This section describes key features, system block diagram and system mechanical outline for S9501 Series.

4.1 Feature Summary

- Ethernet I/O ports:
  S9501-28SMT:
  - 4 x 100M/1GbE RJ45 ports
  - 16 x 100M/1G/2.5GbE SFP ports
  - 6 x 1G/2.5G/10GbE SFP+ ports
  - 2 x 1G/10GbE SFP+ ports with MACSec option

  S9501-18SMT:
  - 4 x 100M/1GbE RJ45 ports
  - 8 x 100M/1G/2.5GbE SFP ports
  - 6 x 1G/2.5G/10GbE SFP+ ports
- Front/Real panel LED indicators:
  - 1 x power status LED
  - 1 x fan status LED
  - 1 x system status LED
  - 1 x synchronization status LED
  - 1 x GNSS\GPS status LED
  - Per port FAN status LED
  - Per port PSU status LED
  - Per port link status LED
- Management interfaces:
  - 1 x GbE OOB management port (CPU/BMC)
  - 1 x USB2.0 Type-A general purpose port
  - 1 x RS232 console port in RJ45 form factor
  - 1 x tact switch for system reset/reload default configuration
- Timing Synchronization:
  - 1588V2 and SyncE with T-GM, T-TC, T-BC support
  - Input source : GNSS, E1/T1**(S9501-28SMT only)**, ToD(RJ45), 1PPS(SMB) and 10MHz(SMB)
  - Output source : ToD(RJ45), 1PPS(SMB) and 10MHz(SMB)

4.2 Component Summary

- PCBA:
  - 1 x Switch board (BOM option will be vary based on SKU definition)
  - 1 x CPU card
  - 1 x FAN card
  - 1 x NTM card
  - 1 x BMC card
  - 1 x PSU card
- On board key components:
  - Switch Board
    - 1 x Q-UX MAC:
      - **S9501-28SMT:** BCM88270,
      - **S9501-18SMT:** BCM88272,
    - 2 x 512MB DDR4 SDRAM @ 800MHz

- 1 x Dual port 10GbE PHY BCM82759 (**S9501-28SMT only)**
- 1 x Quad port 1GbE PHY BCM54140
- 1 x management CPLD 10M04SAU324I7G
- 1 x PCIe/NCSI NIC I210-IT for CPU & BMC
- 1 x Clock jitter attenuator buffer Si5344D
- 1 x Clock Generator ZL30262LDG1
- 1 x GNSS module NEO-M8T
- 1 x T1/E1 transceiver 82P2281 (**S9501-28SMT only)**
- 1 x 32GB M.2 SSD memory module

■ CPU Card

- 1 x CPU Denverton-NS C3508 with two/four cores @ 1.6GHz
- 1 x 8GB DDR4 SODIMM memory module with ECC support

● PSU Card:

- 2x 200W slim PSUs with redundancy support

● FAN Card:

- 3x FAN tray modules with 2+1 redundancy support

● Timing Card:

- 1x DPLL ZL30773 or ZL30795
- 1x FPGA M2GL005VFG256I

● BMC Card:

- 1x AST2600A1 or AST2620A2

4.3 Switch Board Functional Block Diagram

S9501 Series system functional block diagram is shown as below:

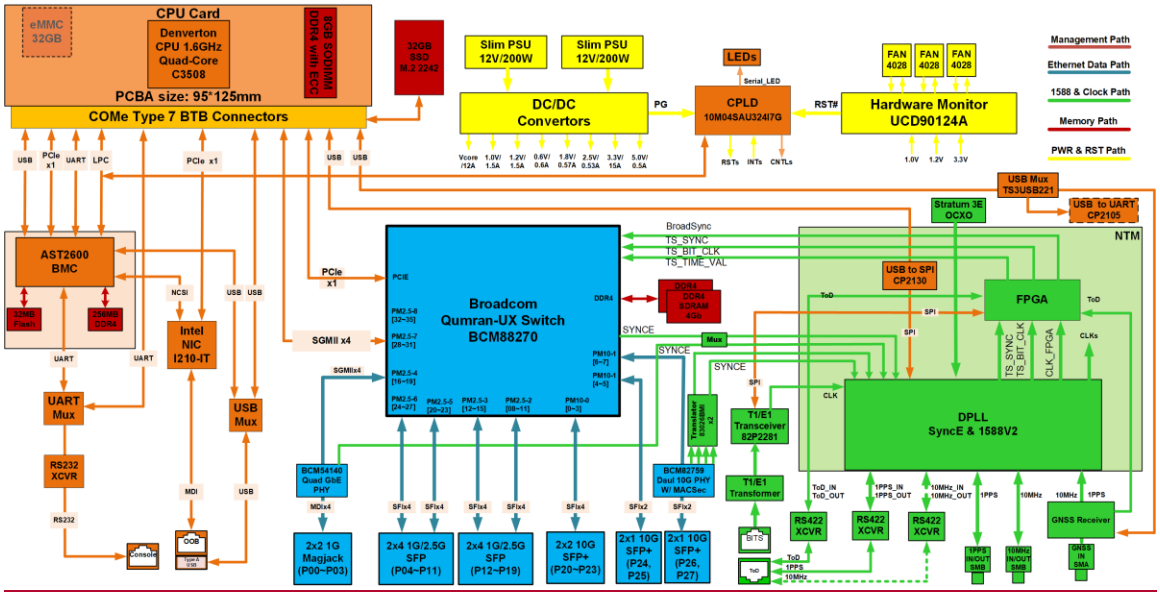


Figure 4-1 S9501-28SMT Switch Board Block Diagram

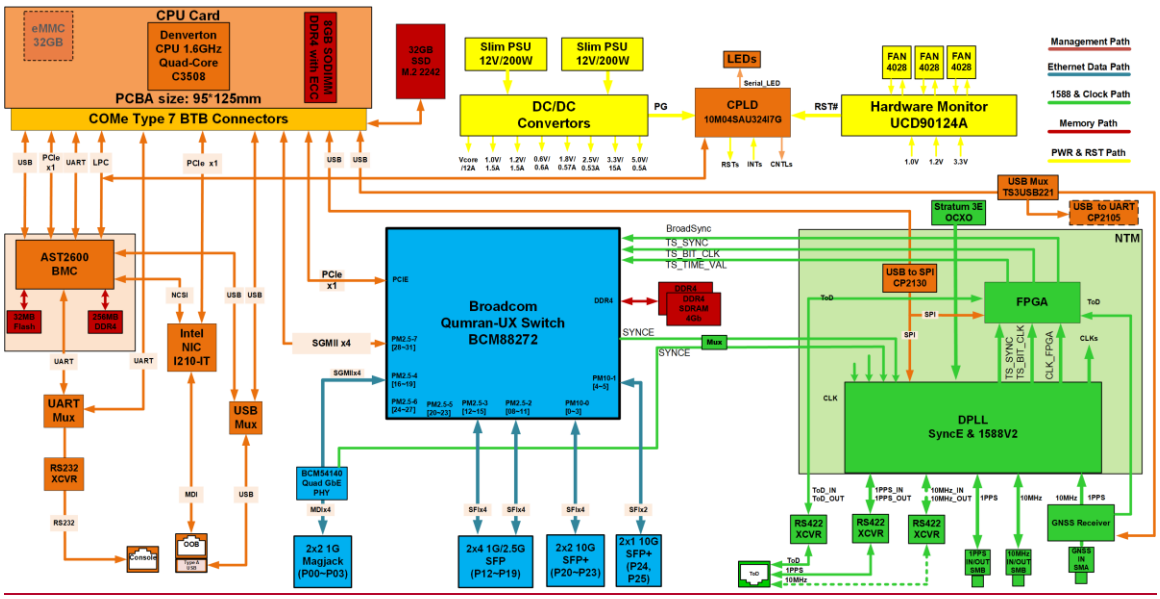


Figure 4-2 S9501-18SMT Switch Board Block Diagram

DCSG Lite switch main board placement is shown as below, parts highlighted in yellow are installed on PCB top side while components in blue are stuffed on bottom side, all SKUs share the same PCB design, with different BOM options:

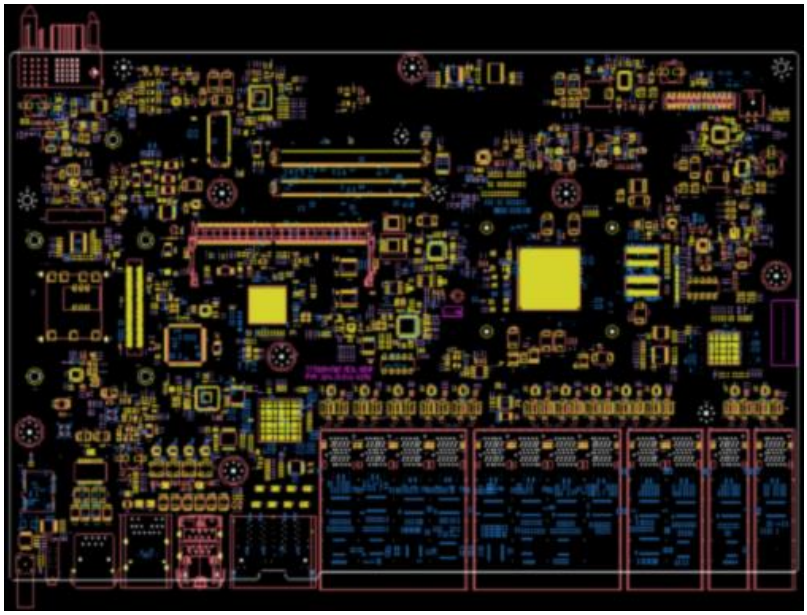


Figure 4-3 DCSG Lite Switch Board PCB Layout

Main Board	Inches	Millimeters
Width	12.2	310
Depth	8.26	210

Table 4-1 Switch Board Dimension

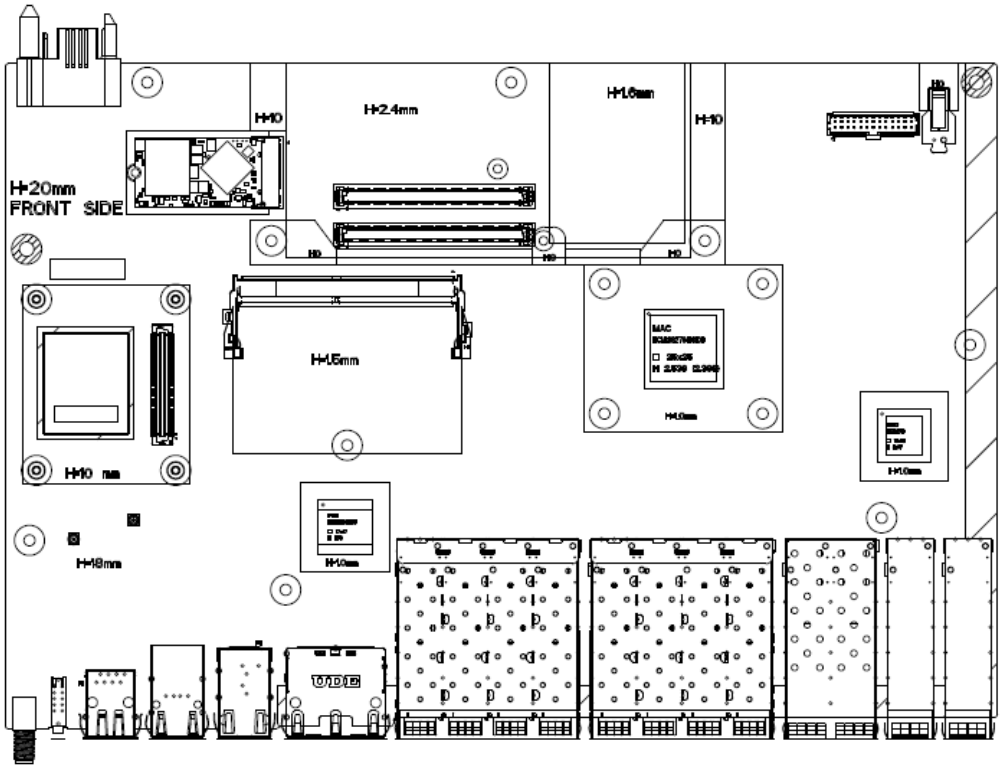


Figure 4-4 DCSG Lite Switch Board Dimension

4.4 CPU Card Functional Block Diagram

The S9501 Series CPU card block diagram is shown as below:

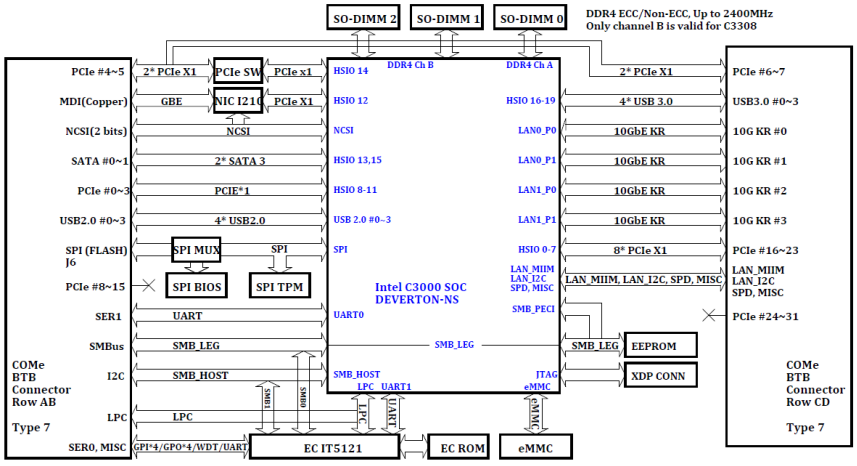


Figure 4-5 CPU Board Functional Block Diagram

The S9501 Series CPU card placement is shown as below:

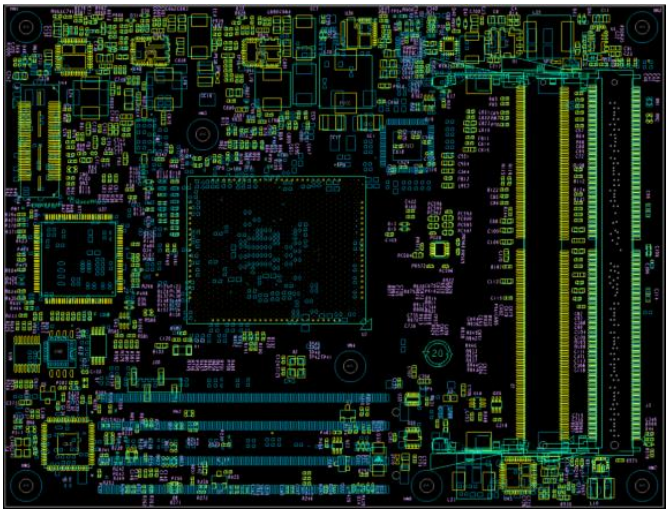


Figure 4-6 CPU Board PCB Layout

Main Board	Inches	Millimeters
Width	4.9	125
Depth	3.54	90

Table 4-2 CPU Board PCB Dimension

4.5 Mechanical Outline

The S9501 Series chassis is designed to meet cabinet with 19'' depth installation requirement. This 1RU system mechanical dimension is: 440mm (W) x 302mm (D) x 43.5mm (H).

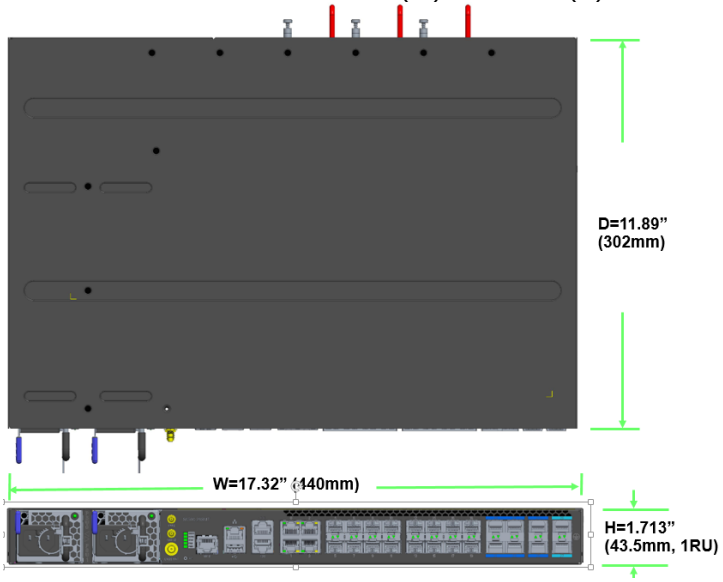


Figure 4-7 DCSG Lite Mechanical Outline

Note: Mechanical outline including front panel is for illustration only, different SKUs comes with different mechanical design and I/O configurations.

4.6 System Explode Diagram

Below shows the S9501 Series system explode view, main board will be populated into the base chassis and then follow by FAN control board, air baffle together with MB, FAN card will be fixed by screw. Next step CPU card will be installed into the dual 440 pin BTB connectors and being fixed with standoff/screw. FAN and PSU modules will be plugged into FAN & PSU slots after chassis top cover is fixed.

Below figures show S9501-28SMT system explode plot for illustration purpose, S9501-18SMT come with the same architecture but with different chassis, mainboard and/or PSU FRU.

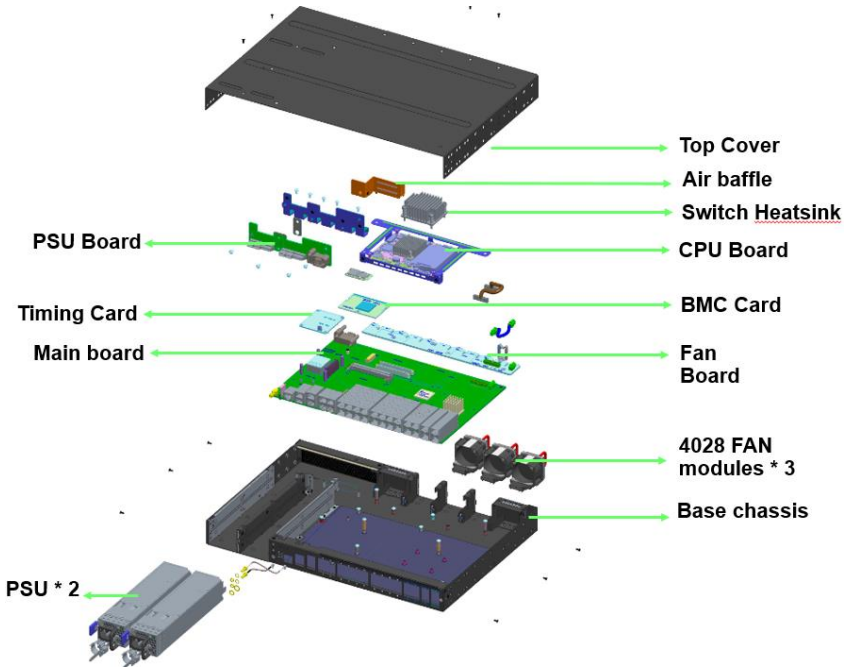


Figure 4-8 S9501 Series System Explode Plot

S9501 Series system top view without top cover is shown as below:

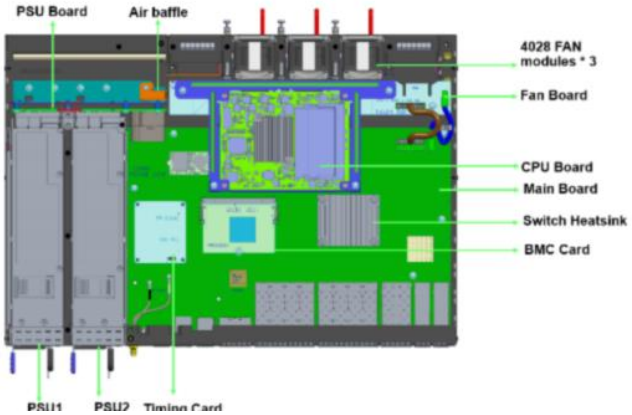


Figure 4-9 S9501 Series System Top View

5 Hardware Architecture

This section describes major components used on the S9501-Series.

5.1 CPU Subsystem

S9501 Series CPU subsystem is designed as standalone module follow COMe Type 7 BTB pinout and 125x95mm PCBA dimension. Intel's Atom embedded SoC processor Denverton-NS C3308 or C3508 is equipped on S9501 Series CPU board. The major onboard components and interfaces to switch board is listed as below:

- Key Components
  - ✓ Denverton-NS CPU supporting up to 2/4-core
  - ✓ One DDR4 ECC SO-DIMMs, up to 8GB
  - ✓ One 32GB M.2 SSD flash module
  - ✓ One 16MB SPI boot/BIOS flash
- Two 220PIN BTB connectors to switch board
  - ✓ Three groups of PCIe lanes
  - ✓ Four 1G/2.5Gbps Ethernet interfaces
  - ✓ One LPC interface
  - ✓ Four USB interfaces
  - ✓ Two SATA interfaces
  - ✓ Two UART interfaces
  - ✓ Two SMBus interfaces

5.2 BMC Subsystem

In S9501 Series, baseboard management controller (BMC) is designed as standalone module follow RunBMC pinout and form factor, it autonomous monitors system's health including temperature, voltage, PSU, fan FRU monitoring and fan speed control, etc.

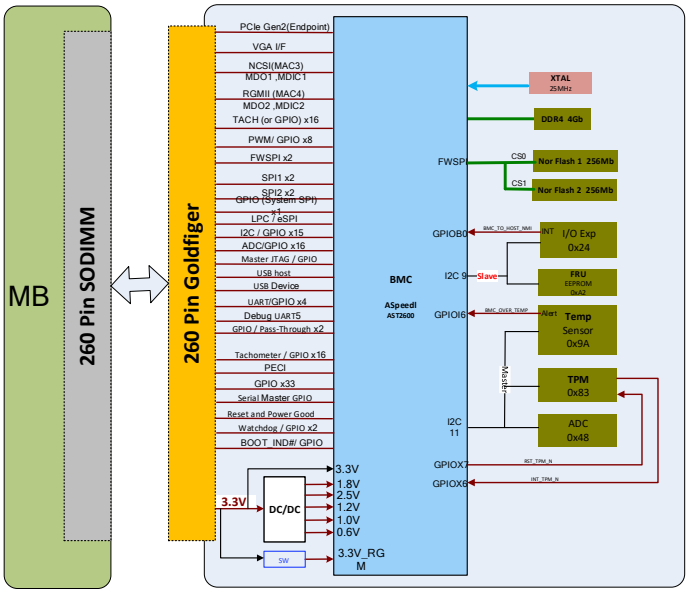


Figure 5-1 BMC Block Diagram

S9501 Series BMC card placement is shown as below:

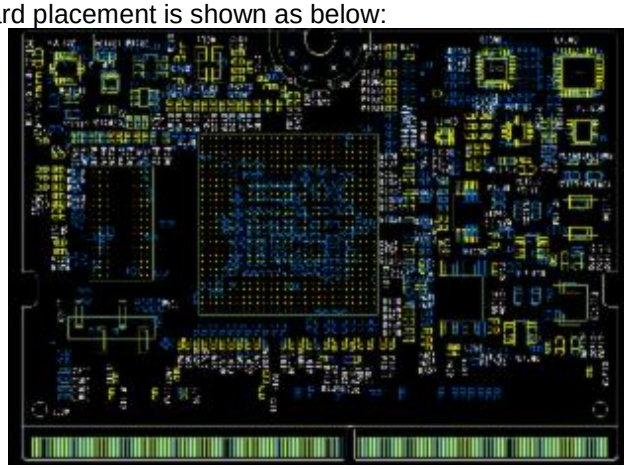


Figure 5-2 BMC Board PCB Layout

5.2.1 Aspeed AST2620

AST2600/AST2620 is the 7th generation of Integrated Remote Management Processor introduced by ASPEED Technology Inc. It is a vastly integrated SOC device playing as a service processor to support various functions required for highly manageable server platforms. In this generation, the CPU performance is improved significantly by integrating 1.2GHz dual cores ARM Cortex A7 processor with FPU. Additionally, most of the controllers are improved with more features or performance. AST2600/AST2620 also support more interfaces like support PCIe Gen2 root complex which can make BMC to have expended control capacity. Finally, real secure boot function with secure OTP memory can improve the BMC security.

Differences between AST2600 & AST2620 is the AST2600 comes with VGA and KVM feature, which is designed for GUI application used on server platforms, AST2620 with VGA and KVM features removal is suitable for networking application.

Features summary:

- Dual-core ARM Cortex A7 CPU, max running frequency to 1.2GHz
- 1x Firmware SPI memory controller with 256MB of direct SPI addressing
- 1x DDR4 memory controller with 1Gbx16 DRAM supported
- 4x 10/100/1000 Mbps Fast Ethernet MAC with RMII/RGMII/NCSI supported
- 12x multi-function I2C/SMBus controller supports either master or slave mode
- 2x USB1.1 UHCI, USB 2.0 Host Controller or 2x USB Device
- 13x UART(16550) with UART5 for firmware console
- 2x System SPI Memory Controller
- 1x PCI-Express 1x Bus Root Complex
- 1x PCI-Express 1x Bus End Device
- 1x LPC Bus Interface or eSPI
- 1x Super I/O Controller
- 16x ADC inputs with 10bit resolution
- 16x PWM outputs with 1/256 resolution
- 16x tachometer inputs

- 1x PECI Controller

5.2.2 LPC Bus

Low-pin-count interface is an important interface for communication among Denverton-NS, CPLD and BMC. The OS running on x86 uses this interface to communicate with BMC through IPMI message handler. LPC base address for CPU EC is 0xe300, for MB CPLD is 0x700, for BMC is 0xCA2(IPMI), 0x2E/2F(SIO).

5.2.3 USB

AST2600 provides two USB interfaces for different functional objectives. The four USB controllers of AST2600 meet USB specification revision 2.0 and 1.1 and also compliant with EHCI and UHCI specification.

5.2.4 GbE MAC

AST2600 integrates two MACs compliant with IEEE802.3 and IEEE802.3z specification. And the transfer rate is up to 10/100/1000M bps. BMC shares the same RJ45 management port in front-panel by connecting NC-SI interface to Intel I210 controller's NC-SI. Software can disable NC-SI if needed.

In system shutdown mode, BMC works and can be accessed by RJ45 console port only, OOB port connection is lost in this case.

5.2.5 UART Bus

AST2600 supports up to 13 sets UART IO interface with full flow control pins, and 1 set(UART5) with Tx/Rx only for BMC console. The administrator can switch x86 and BMC console easily and choose to connect to front panel console RJ45. Also, disabling BMC console is allowed by BIOS setting.

5.2.6 I2C Bus

AST2600 integrates up to 16 sets of multi-function I2C/SMBus bus controllers. In DCSG Lite switch, BMC use 6x I2C interfaces to collect temperature, fan speed, FRU, and manufacture information. BMC continues to monitor system's health after it boots up. And BMC should record and handle the event if sensor's value is over the reasonable range.

5.2.7 GPIO

AST2600 Integrates one set of Parallel GPIO Controller with maximum 244 control pins, which are 31 sets, to provide general-purpose input/output functions. All functional parallel GPIOs of S9501 Series in different group are listed as below, net names ended with '_N' means this signal is active low, otherwise it's active high or it's a mux select pin.

5.2.8 Watchdog Timer/Keep Alive

AST2600 has two build-in sets of 32-bit WDT modules. In the S9501 Series, we use WDT to keep alive with x86 system. The OS running in x86 can enable watchdog timer, set timeout counter, and timeout behavior by using IPMI command. If OS was halted, BMC would reset x86 system after watchdog timer expired.

5.2.9 SPI Boot Flash

There are two 64MB (512Mb) SPI boot flashes for AST2600 U-boot, which are stuffed on main board. It's used for BMC OS and application software storage. In manufacture, both of these two components store the same BMC image. By default, system boots from primary SPI flash (CS0#). It will swap to backup SPI flash (CS#1) when system boot up fail from primary flash.

Dual boot flash design is also useful for BMC firmware upgrade, in the case of the flash is crash during firmware upgrade, it will be recovered by the original image stored in the backup flash.

5.2.10 DDR3 SDRAM

The memory controller unit integrated in AST2600 supports x16 data bus width DDR4 SDRAM. One 256Mb x16 DDR4 SDRAM is installed for AST2600.

5.3 Switching Subsystem

This section details switch board component features/functionalities summary and hardware system design.

5.3.1 MAC Component -- BCM88270

The Broadcom® BCM88270 series is a member of the centralized switching solutions family from the StrataDNX product line.

The BCM88270 series of devices processes up to 120 Gb/s traffic at Layer 2 through Layer 4, with integrated deep-buffer traffic management capabilities. The BCM88270 family has integrated 1GbE, 2.5GbE, 10GbE, and 40GbE MAC network interfaces, supporting various port rate combinations.

The BCM88270 series expands the reach of networking solutions based on StrataDNX to the very edge of the carrier network, allowing for power-sensitive and cost-sensitive applications with lower capacity to leverage all the functional and architectural benefits of the high-scale StrataDNX family, such as deep packet buffers, hierarchical scheduling, and a flexible packet processor −all in a highly integrated SoC.

The BCM88270 traffic manager integrates deep packet buffers with state-of-the-art hierarchical QoS, transmission scheduling, and flow control. These advanced scheduling and queuing schemes natively support all the latest innovations in data center networking, such as PFC, ETS, delay-based ECN, and overlay networks, allowing per-customer/per-service scheduling in carrier access/aggregation switches.

Industry grade BCM88270IFSBG is adopted on S9501 Series.

5.3.1.1 Features Summary

- High-performance:
  - 120 Gb/s full-duplex integrated traffic manager and packet processor.
  - 125 Mpps processing rate.
- Flexible network interface:
  - Total of 36 SerDes.
  - Pool of 8 SerDes at up to 10.3 Gb/s each; flexible assignment to protocols.
  - Supported protocol blocks for the 10.3G SerDes:
    - ✓ 8 ×1GbE/2.5GbE over SGMII/1000BASE-X (1000BASE-X may use SFI).
    - ✓ 8 x 10GbE over 10GBASE-R (may use SFI+ and KR).
    - ✓ 2 x 10GbE over XAUI.
    - ✓ 4 x 10GbE over RXAUI.
    - ✓ 2 x 40GbE over XLAUI 4-lane.
  - Pool of 28 SerDes at up to 3.125 Gb/s each.
  - Supported protocol blocks for the 3.125G SerDes:
    - ✓ 28 x GbE over SGMII/1000BASE-X.
    - ✓ 7 x 10GbE over XAUI.
  - Packets lengths supported in the range 64B‑10KB.
- Traffic Manager:
  - 16K programmable wire-rate queues.
  - Deep buffering: 8Gb DRAM-based.
  - Congestion management:
    - ✓ Hierarchical WRED and tail drop policies.
    - ✓ Flow Control generation: fully programmable, in-band and out-of-band.
    - ✓ Flow Control reception-any level: interface, port, class, flow, traffic type-in-band and out-of band.
    - ✓ Priority Flow Control (PFC): eight levels.
    - ✓ Congestion tracking statistics.
  - Hierarchical scheduling and shaping: fully programmable to any depth.
  - MEF, DSL-FORUM TR-059-compliant scheduling and shaping.
  - Ingress shaping: efficient with pointer manipulation only.
- Packet processor:
  - Metro Ethernet, enterprise, and data center.
  - Large on-chip databases.
  - Full-featured: bridging, routing, MPLS, VPLS, L2VPNs, L3VPNs, OAM, and so on.
  - Microcode controlled hardware: flexible and future-proof
- Multicast: pointer-based ingress and/or egress multicast replication.
- Statistics interface: expandable, off-chip statistics gathering:
  - SerDes-based: The SerDes used for the statistics interface is shared with the NIF SerDes.
  - Efficient packet-based protocol: simplifies connectivity to FPGAs.
- In-band management.
- PCIe x1 lanes Gen 2 host interface with DMA.
- IPsec engine:

- Internal security module to support IPsec tunnel initiation and termination.
- IPsec tunnel mode (ESP).
- Encryption/decryption performance up to 8 Gb/s.
- Encryption algorithms:
  - ✓ AES-128-CBC.
- Authentication algorithms:
  - ✓ SHA-1.
- Up to 384 SA/tunnels (unidirectional).

5.3.2 Network Port Design

This section describes the data path for each Ethernet fiber, copper port and the management path for each PHY.

5.3.2.1 Network Port Path Configuration

This section shows the physical port location assignment and Ethernet data path.

5.3.2.1.1 Port Assignments

BCM88270 is adopted in S9501-28SMT, which contains 4x 100M/GE RJ45 copper ports, 16x 100M/1GE/2.5GE SFP ports, 8x GE/2.5GE/10GE SFP+ ports, port 27 & 28 with external PHY BCM82759 equipped supports MACSec feature, front panel I/O ports numbering is shown as below:



Figure 5-3 DCSG Lite -- S9501-28SMT Front Panel

BCM88272 is adopted in S9501-18SMT, which contains 4x 100M/GE RJ45 copper ports, 8x 100M/1GE/2.5GE SFP ports, 6x 1GE/2.5GE/10GE SFP+ ports, front panel I/O ports numbering is shown as below:



Figure 5-4 DCSG Lite -- S9501-18SMT Front Panel

The table below shows the network ports numbering and speed.

Function	Port#	Speed	Notes
RJ45 Copper Ports	P0	100M/1G	SyncE supported
	P1	100M/1G	SyncE supported
	P2	100M/1G	SyncE supported
	P3	100M/1G	SyncE supported
SFP Ports	P4	100M/1G/2.5G	PHY-less port , ZR optics capable
	P5	100M/1G/2.5G	PHY-less port , ZR optics capable
	P6	100M/1G/2.5G	PHY-less port , ZR optics capable

Function	Port#	Speed	Notes
	P7	100M/1G/2.5G	PHY-less port , ZR optics capable
	P8	100M/1G/2.5G	PHY-less port , ZR optics capable
	P9	100M/1G/2.5G	PHY-less port , ZR optics capable
	P10	100M/1G/2.5G	PHY-less port , ZR optics capable
	P11	100M/1G/2.5G	PHY-less port , ZR optics capable
	P12	100M/1G/2.5G	PHY-less port , ZR optics capable, 28SMT only
	P13	100M/1G/2.5G	PHY-less port , ZR optics capable, 28SMT only
	P14	100M/1G/2.5G	PHY-less port , ZR optics capable, 28SMT only
	P15	100M/1G/2.5G	PHY-less port , ZR optics capable, 28SMT only
	P16	100M/1G/2.5G	PHY-less port , ZR optics capable, 28SMT only
	P17	100M/1G/2.5G	PHY-less port , ZR optics capable, 28SMT only
	P18	100M/1G/2.5G	PHY-less port , ZR optics capable, 28SMT only
	P19	100M/1G/2.5G	PHY-less port , ZR optics capable, 28SMT only
SFP+ Ports	P20	1G/10G	PHY-less port , ZR optics capable
	P21	1G/10G	PHY-less port , ZR optics capable
	P22	1G/10G	PHY-less port , ZR optics capable
	P23	1G/10G	PHY-less port , ZR optics capable
	P24	1G/10G	PHY-less port , ZR optics capable, 18SMT, 28SMT only
	P25	1G/10G	PHY-less port , ZR optics capable, 18SMT, 28SMT only
	P26	1G/10G	MACSec supported, ZR optics capable, 28SMT only
	P27	1G/10G	MACSec supported, ZR optics capable, 28SMT only

Table 5-1 Network Port Connection

5.3.2.1.2 *Copper and Optical Ports Data, Management Path*

RJ45 port 0~3 driven by 1G PHY BCM54140, which is managed by MAC through MIIM0, SFP+ port 26~27 are re-driven by 10G PHY BCM82759, which is managed by MAC through MIIM2. All other SFP+/SFP+ ports are PHY-less design.

Table below shows the network ports data and MIIM management path of S9501-28SMT:

<table>
<tr><th colspan="2">Front Panel</th><th colspan="4">PHY</th><th colspan="4">MAC</th></tr>
<tr><th>Function</th><th>Port#</th><th>DEVICE</th><th>Lane#</th><th>MIIM</th><th>MIIM ADDR</th><th>DEVICE</th><th>SerDes Core</th><th>Lane#</th><th>Interface</th></tr>
<tr><td rowspan="4">RJ45 Ports</td><td>P0</td><td rowspan="4">BCM54140</td><td>0</td><td rowspan="4">M0</td><td>00000</td><td rowspan="20">MAC BCM88270</td><td rowspan="4">PM2.5-4 [16~19]</td><td>19</td><td rowspan="4">SGMII</td></tr>
<tr><td>P1</td><td>1</td><td>00001</td><td>18</td></tr>
<tr><td>P2</td><td>2</td><td>00010</td><td>17</td></tr>
<tr><td>P3</td><td>3</td><td>00011</td><td>16</td></tr>
<tr><td rowspan="16">SFP Ports</td><td>P4</td><td colspan="5" rowspan="16">MAC Internal SerDes</td><td rowspan="4">PM2.5-6 [24~27]</td><td>27</td><td rowspan="16">SFI</td></tr>
<tr><td>P5</td><td>26</td></tr>
<tr><td>P6</td><td>25</td></tr>
<tr><td>P7</td><td>24</td></tr>
<tr><td>P8</td><td rowspan="4">PM2.5-5 [20~23]</td><td>23</td></tr>
<tr><td>P9</td><td>22</td></tr>
<tr><td>P10</td><td>21</td></tr>
<tr><td>P11</td><td>20</td></tr>
<tr><td>P12</td><td rowspan="4">PM2.5-3 [12~15]</td><td>15</td></tr>
<tr><td>P13</td><td>14</td></tr>
<tr><td>P14</td><td>13</td></tr>
<tr><td>P15</td><td>12</td></tr>
<tr><td>P16</td><td rowspan="4">PM2.5-2 [08~11]</td><td>11</td></tr>
<tr><td>P17</td><td>10</td></tr>
<tr><td>P18</td><td>9</td></tr>
<tr><td>P19</td><td>8</td></tr>
</table>

Front Panel		PHY				MAC			
Function	Port#	DEVICE	Lane#	MIIM	MIIM ADDR	DEVICE	SerDes Core	Lane#	Interface
SFP+ Ports	P20	MAC Internal SerDes				MAC BCM88270	PM10-0 [0~3]	1	SFI
	P21							0	
	P22							2	
	P23							3	
	P24						PM10-1 [4~5]	5	
	P25							4	
SFP+ Ports	P26	BCM82759	0	M2	00000	MAC BCM88270	PM10-1 [6~7]	7	XFI
	P27		1		00001			6	
CPU MAC	Lane0					MAC BCM88270	PM2.5-7 [28~31]	28	2500BASE -X
	Lane1							29	
	Lane2							30	
	Lane3							31	

Table 5-2 S9501-28SMT Network Port Connection

Table below shows the network ports data and MIIM management path of S9501-18SMT:

Front Panel		PHY				MAC			
Function	Port#	DEVICE	Lane#	MIIM	MIIM ADDR	DEVICE	SerDes Core	Lane#	Interface
RJ45 Ports	P0	BCM54140	0	M0	00000	MAC BCM88272	PM2.5-4 [16~19]	18	SGMII
	P1		1		00001			19	
	P2		2		00010			16	
	P3		3		00011			17	
SFP Ports	P4	MAC Internal SerDes					PM2.5-3 [12~15]	15	SFI
	P5							14	
	P6							13	
	P7							12	
	P8						PM2.5-2 [08~11]	11	
	P9							10	
	P10							9	
	P11							8	
SFP+ Ports	P12	MAC Internal SerDes				MAC BCM88272	PM10-0 [0~3]	1	SFI
	P13							0	
	P14							2	
	P15							3	
	P16						PM10-1 [4~5]	5	
	P17							4	
CPU MAC	Lane0					MAC BCM88272	PM2.5-7 [28~31]	28	2500BASE -X
	Lane1							29	
	Lane2							30	
	Lane3							31	

Table 5-3 S9501-18SMT Network Port Connection

5.4 Timing Subsystem

This chapter describes timing subsystem of the S9501 Series. There are two clock domains:

- Local clock for non-synchronized components (BMC, I210, DDR4, etc)
- Network timing clock for synchronized Ethernet components: MAC, PHY

Local clock sources are generated by motherboard clock generator ZL30262, while the synchronized clocks are generated by NTM (Network Timing Module).

5.4.1 Local Clock Sources of System

Components, like BMC, NIC i210, DDR4, PCIe Bus and core/DDR clocks of Qumran-UX have separate clock domain and don't synchronize timing from PTP or SyncE recovered clock. These clocks will be generated by ZL30262 right after system power on and don't need to have further software configuration.

5.4.2 Network Timing Synchronization Subsystem

The other subsystem is for network timing synchronization, it is a key subsystem that enables the S9501 Series to synchronize to external clock or timing sources, including 1588 packet, SyncE recovered clock, GNSS, ToD, BITS, 1PPS, 10M reference sources.

5.5 Fan and PSU Cards

5.5.1 FAN and PSU Card Placements

Fan Card

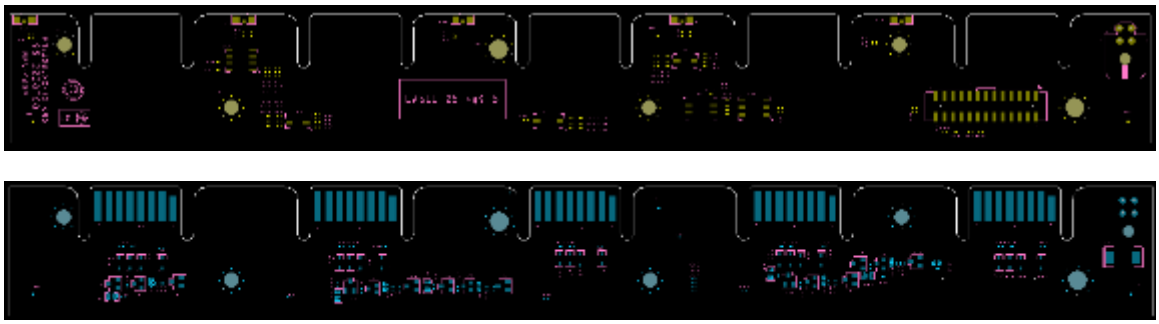


Figure 5-5 Fan Card PCB Placement

PSU Card

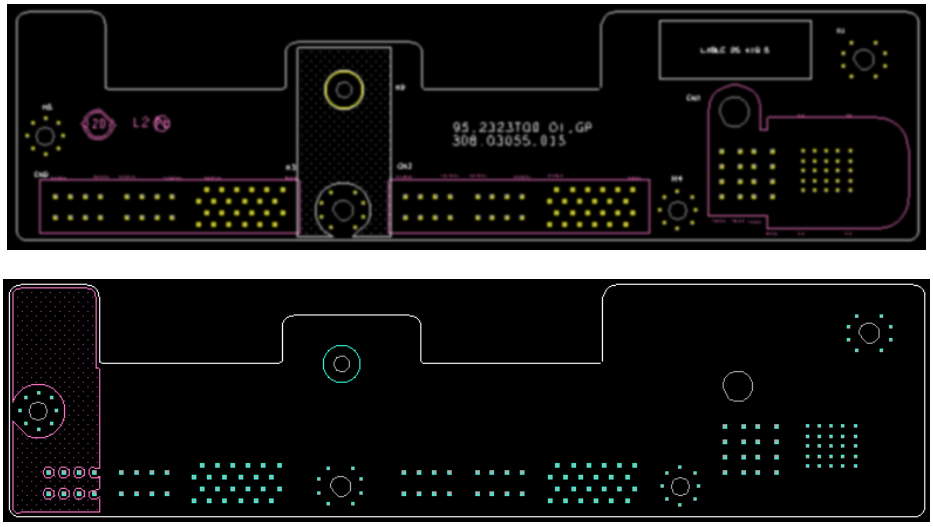


Figure 5-6 PSU Card PCB Placement

5.5.2 FAN and PSU Card Dimensions

Fan Card

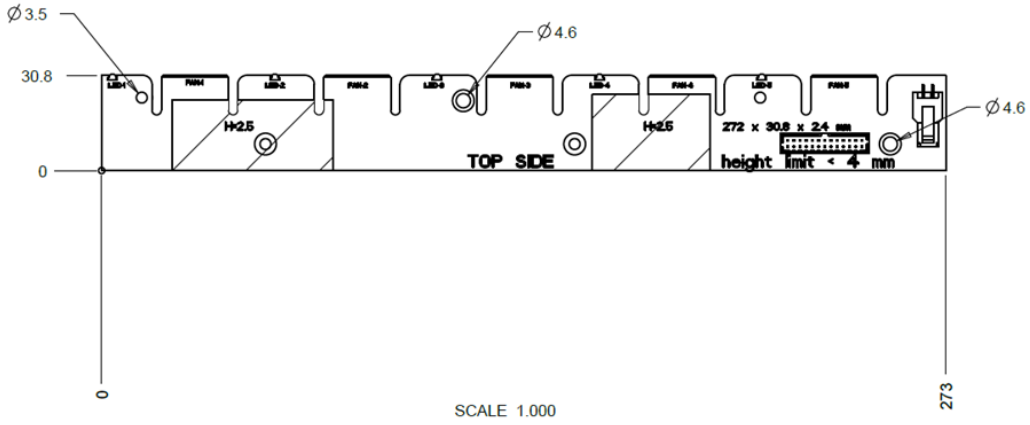


Figure 5-7 Fan Card PCB Dimension

PSU Card

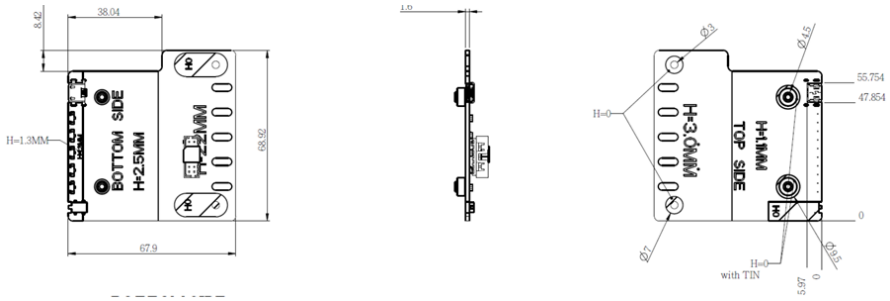


Figure 5-8 PSU Card PCB Dimension

5.6 Front Panel Design

The S9501 Series front panel IO ports include below functionalities:

- System status LED
  - ✓ Power status LED
  - ✓ FAN status LED
  - ✓ GNSS status LED
  - ✓ Synchronization status LED
- Ethernet ports LED
  - ✓ OOB copper ports LED
  - ✓ Data traffic fiber ports LED
- Management ports (Share between CPU and BMC)
  - ✓ 1x OOB port
  - ✓ 1x Type A USB port
  - ✓ 1x console port in RJ45
- Ethernet data ports
  - ✓ 4x 100M/GE RJ45 ports

- ✓ 16x 1G/2.5G SFP ports
- ✓ 8x 10G SFP+ ports

- ● Timing synchronization ports
- ✓ 1x GNSS port with SMA connector
- ✓ 1x T1/E1 port with RJ45 form factor
- ✓ 1x ToD port with RJ45 form factor
- ✓ 2x SMB ports with 1PPS and 10MHz input/output

Detailed IO arrangement is shown as below:

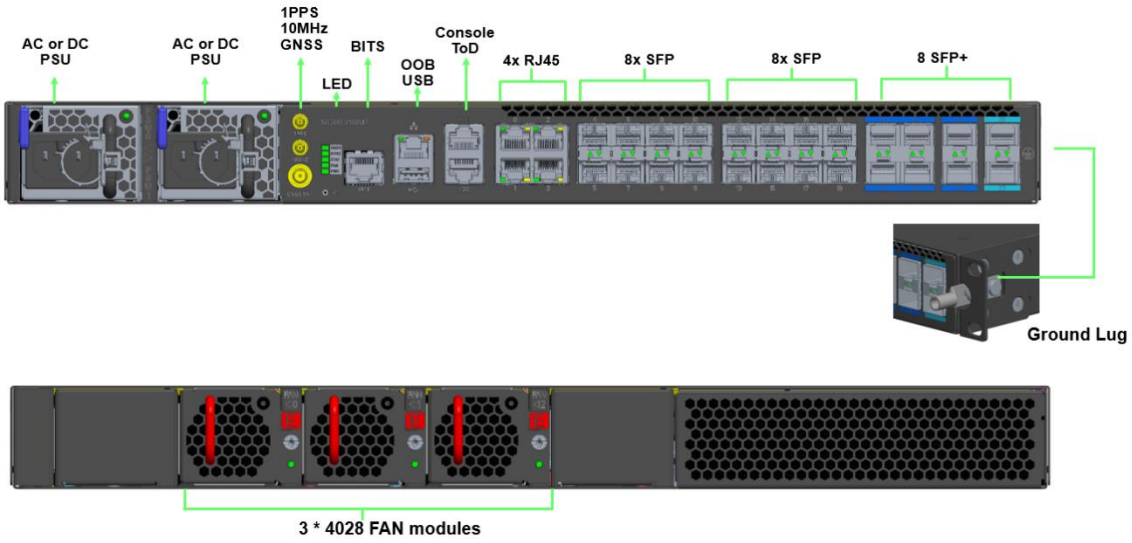


Figure 5-9 Front Panel IO Arrangement

5.6.1 System LED Indicators

The front panel system status LED are placed on Main board.

LED Function/State	Meaning	Comment
PWR (Green/Yellow): controlled by CPLD LED Interface Bit [0:1]		
OFF	No power or in shutdown mode.	Bit [0]=1; Bit [1]=1
Solid Green	System power good & BMC is present & BMC power good	Bit [0]=0; Bit [1]=1
Blinking Green (1Hz on / 1Hz off)	System power good & BMC is present but BMC power fail	Bit [0]=0; Bit [1]=**B**
Solid Yellow	System power good & BMC is absent	Bit [0]=1; Bit [1]=0
Blinking Yellow (0.5Hz)	System power fail	Bit [0]=**B**; Bit [1]=0
FAN (Green/Yellow): controlled by CPLD LED Interface Bit [2:3]		
OFF	Reserved	Bit [0]=1; Bit [1]=1
Solid Green	All FAN modules work well	Bit [0]=0; Bit [1]=1

LED Function/State	Meaning	Comment
Blinking Green	Reserved	Bit [0]=0; Bit [1]=**B**
Solid Yellow	Reserved	Bit [0]=1; Bit [1]=0
Blinking Yellow	One or more FAN module(s) fail or no FAN module present	Bit [0]=**B**; Bit [1]=0
STAT (Green/Yellow): controlled by CPLD LED Interface Bit [4:5]		
OFF	System (X86 & BMC) no boot	Bit [2]=1; Bit [3]=1
Solid Green	System boot complete (NOS) **Note: need NOS to integrate this feature	Bit [2]=0; Bit [3]=1
Blinking Green	System is booting	Bit [2]=**B**; Bit [3]=1
Solid Yellow	System boot complete (DIAG OS)	Bit [2]=1; Bit [3]=0
Blinking Yellow	Reserved	Bit [0]=**B**; Bit [1]=0
GNSS (Green/Yellow): controlled by CPLD LED Interface Bit [8:9]		
OFF	GNSS is not configured. **Note: need NOS to integrate this feature	Bit [8]=1; Bit [9]=1
Solid Green	GNSS is in normal state. Self-survey is complete. **Note: need NOS to integrate this feature	Bit [8]=0; Bit [9]=1
Blinking Green	GNSS is in learning state. Self-survey is not completed. **Note: need NOS to integrate this feature	Bit [8]= **B**; Bit [9]=1
Solid Yellow	Power up. GNSS is not tracking any satellite. **Note: need NOS to integrate this feature	Bit [8]=1; Bit [9]=0
Blinking Yellow	GNSS antenna is short to ground. **Note: need NOS to integrate this feature	Bit [8]= **B**; Bit [9]=1
SYNC (Green/Yellow): controlled by CPLD LED Interface Bit [10:11]		
OFF	System timing synchronization is disabled or in free-run mode. **Note: need NOS to integrate this feature	Bit [10]=1; Bit [11]=1
Solid Green	System timing core(1588 and SyncE) is synchronized to external timing source (ex: GNSS, 1PPS, PTP, BITS, etc) **Note: need NOS to integrate this feature	Bit [10]=0; Bit [11]=1
Blinking Green	System is synchronized in SyncE mode. **Note: need NOS to integrate this feature	Bit [10]= **B**; Bit [11]=1
Solid Yellow	System timing core is in acquiring state or holdover mode. **Note: need NOS to integrated this feature	Bit [10]=1; Bit [11]=0
Blinking Yellow	System timing synchronization fail. **Note: need NOS to integrated this feature	Bit [10]=1; Bit [11]= **B**
Note : **B**= Blinking, interleaved bit value with 1 and 0		

Table 5-4 System LED Description

PSU LED Function/State	Meaning
OFF	No DC power to all PSUs
Flashing Red	No DC power to this PSU
Flashing Green	DC present, only standby output on. Poor contact

Green	PSU DC output ON and OK
Red	PSU failure.
Flashing between Green and Red	Warning. Working condition not satisfied. Please check the voltage, electric current, and temperature.

Table 5-5 PSU LED Description

Fan LED Function/State	Meaning
OFF	Main board 3.3V power fail or Fan is not present.
Solid Green	Fan is present and interrupt de-assert
Blinking Green	N/A
Solid Yellow	N/A
Blinking Yellow	Fan is present but interrupt assert.

Table 5-6 FAN LED Description

LED Function/State	Meaning	Comment
RJ45 (port 0-3) (Green/Yellow):		
OFF	No link on the RJ45 port	
Solid Green	RJ45 port link at 1G mode	
Blinking Green	RJ45 port is transmitting at 1G mode	
Solid Yellow	RJ45 port link at 10M/100M mode	
Blinking Yellow	RJ45 port is transmitting at 10M/100M mode	
SFP (port 4-19) (Green/Yellow):		
OFF	No link on the SFP port	
Solid Green	SFP port link at 1G mode	
Blinking Green	SFP port is transmitting at 1G mode	
Solid Yellow	SFP port link at 2.5G/100M mode	
Blinking Yellow	SFP port is transmitting at 2.5G/100M mode	
SFP+ (port 20-27) (Green/Yellow):		
OFF	No link on the SFP+ port	
Solid Green	SFP+ port link at 10G mode	
Blinking Green	SFP+ port is transmitting at 10G mode	
Solid Yellow	SFP+ port link at 2.5G/1G mode	
Blinking Yellow	SFP+ port is transmitting at 2.5G/1G mode	
OOB port (Green/Yellow):		
OFF	No link on the OOB port	
Solid Green	OOB port link at 1G mode	
Blinking Green	OOB port is transmitting at 1G mode	
Solid Yellow	OOB port link at 10M/100M mode	

Blinking Yellow	OOB port is transmitting at 10M/100M mode	

Table 5-7 Ethernet Ports LED Description

5.6.2 OOB Ports

The S9501 Series includes 1 standard GE RJ45 port for out of band (OOB) management, share between CPU and BMC. It supports the IEEE 802.3 specification for 10/100/1000Mbps operation.

OOB to BMC can be disabled by BIOS.

I210-IT is powered by main power, not standby power rail, which means that OOB port connection is lost in system shutdown mode.

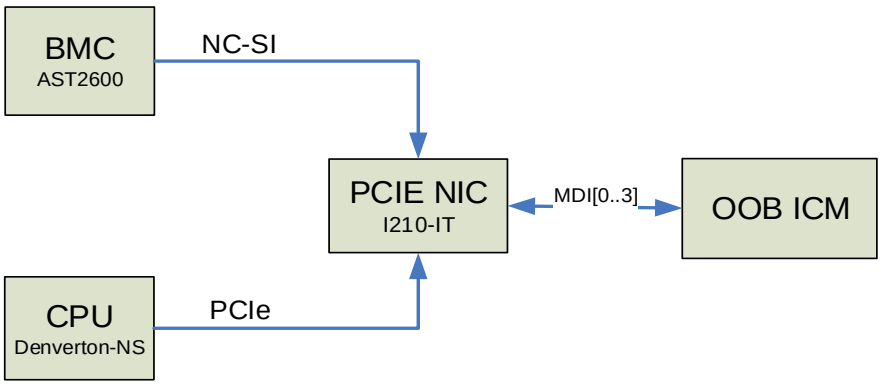


Figure 5-10 CPU OOB Interface Diagram

5.6.3 Console Port

One console port available for DCSG Lite systems access, RS232 console. It can be used for CPU or BMC access. The bound rate is 115200 by default. When either console port cable is plugged, its active immediately, Console port connection diagram is shown as below:

To access the RJ45 RS232 interface, use a RS-232 to RJ45 adapter. The pin definition of the RS232 console port is shown as below.Pin3 is the TX signal from internal processor to external RS232 interface, and Pin6 is the RX signal from external RS232 interface to internal processor.

PIN #	Definition	Direction	Note
1	NC		
2	NC		
3	UART_TXD	Out	Console TX
4	GND		
5	GND		
6	UART_RXD	In	Console RX
7	NC		
8	NC		

Table 5-8 Pin Definition of RJ45 Console Connector

5.6.4 USB 2.0 Port

The S9501 Series integrates a USB 2.0 host controller that supports a single port operating at high speed (HS) at 480 Mbps (USB 2.0).

USB 5V power will be enabled during system initialization, software should de-assert 'USB_PWR_EN' by pulling this pin low once over current event (USB device consumes >0.5A current more than 20mS) is received. 'USB_PWR_EN' need set as 'HIGH' to re-enable USB port.

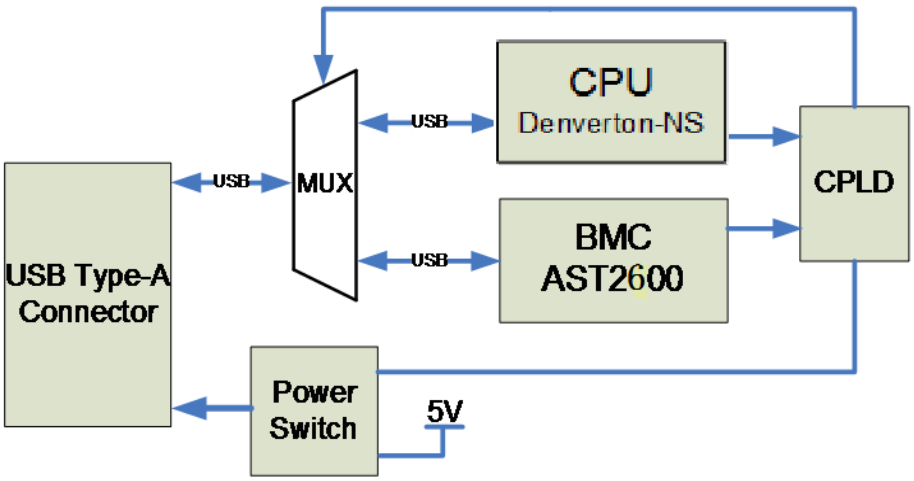


Figure 5-11 USB Interface Diagram

5.6.5 Network Synchronization Ports

- 1x GNSS port with SMA antenna interface
- 1x BITS(T1/E1) port with RJ45 form factor (RJ48 cable)
- 1x ToD port with RJ45 form factor
- 2x SMA ports with 1PPS and 10MHz ref. clock input/output

5.7 Power Consumption

System consumes the maximum power @ 65°C with full traffic loading & all FAN runs at max. 18000RPM. Per measurement, the system power consumption is around 120W with below configuration: timing interface & BMC works normally, 28x port SP/SFP+ loopbacks with 1.5W power, 4x port copper RJ45 loopback, 2x DDR4 SDRAM packet buffer enabled, MAC & 1G, 10G, PHY run at 120Gpbs traffic switching/forwarding, 3x FAN modules runs at 18000RPM.

To consider PSU efficiency 90% from -48V to +12V, overall system power requirement will be 120 / 0.9 = 133.3W.

6 Field Replaceable Components

6.1 Fan Module

New developed FAN tray with 40x40x28mm FAN is adopted on the S9501 Series system to meet chassis depth requirement.

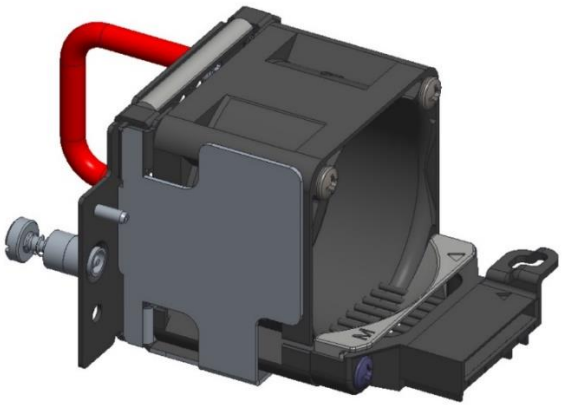


Figure 6-1 4028 FAN Module

6.1.1 Electrical Specifications

Fan module electrical, mechanical and acoustic characteristics are show as below

Rated voltage	12 VDC
Rated current	900mA, 1035mA, max.
Rated power consumption	10.8W, 12.42W, max.
Operating voltage range	10.2~13.2 VDC
Starting voltage	10.2 VDC (25 degC)
Operating temperature	-40~70 degC
Rated speed	18000 RPM+/-10% at rated voltage
Air flow	27.6 CFM max??
Static pressure	2.81 Inch-H2O, 1.96 Inch-H2O min.
Acoustic noise	62.0 dB(A), 69.5 dB(A) max.

Table 6-1 FAN Tray Characteristics

6.1.2 Fan Interface

Molex 46856-0003 wire to gold finger connector is assembled in FAN tray and mated with FAN card gold finger. Following Table 5-2 shows DCSG Lite FAN tray interface pinout.

Pin #	Pin Definition	I/O	Function Description	FAN Tray Connector Connection	FAN Connection
1	+12V	-	FAN 12V power	To inlet, outlet FAN +	Out, +
2	GND	-	FAN GND	To outlet FAN -	Out, -
3	FAN_PRSNT_N	O	FAN module presence signal sent by FAN	Jump to Pin2	PIN 2
4	FAN_PWM_OUTLET	I	Outlet FAN speed PWM control signal from HWM	To outlet FAN PWM	Out, PWM
5	FAN_TACH_OUTLET	O	FAN speed tachometer sent by outlet FAN	From outlet FAN tachometer	Out, 3rd
6					
7					
8					

Table 6-2 Connector Pin Definition of FAN Tray

6.2 Power Supply

The S9501 Series adopts 200W hot swappable power supply unit made by 3Y. Two types of PSU module are supported: One is 110~220Vac input to +12 Vdc output AC/DC PSU, the other one is Neg36~72 V input to +12 Vdc output DC/DC PSU.

6.2.1 Physical Size

The physical size of the power supply enclosure is 40.2mm x 50.5mm x 211mm (height x width x length). The Gold finger height adjustment to 5mm.

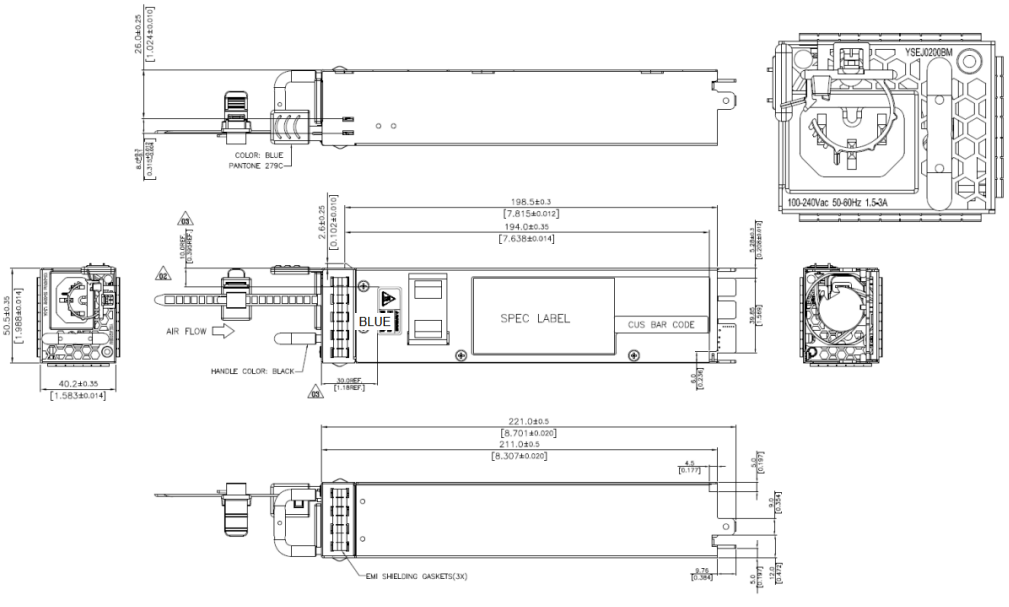


Figure 6-2 System with 200W AC/DC Power Supply

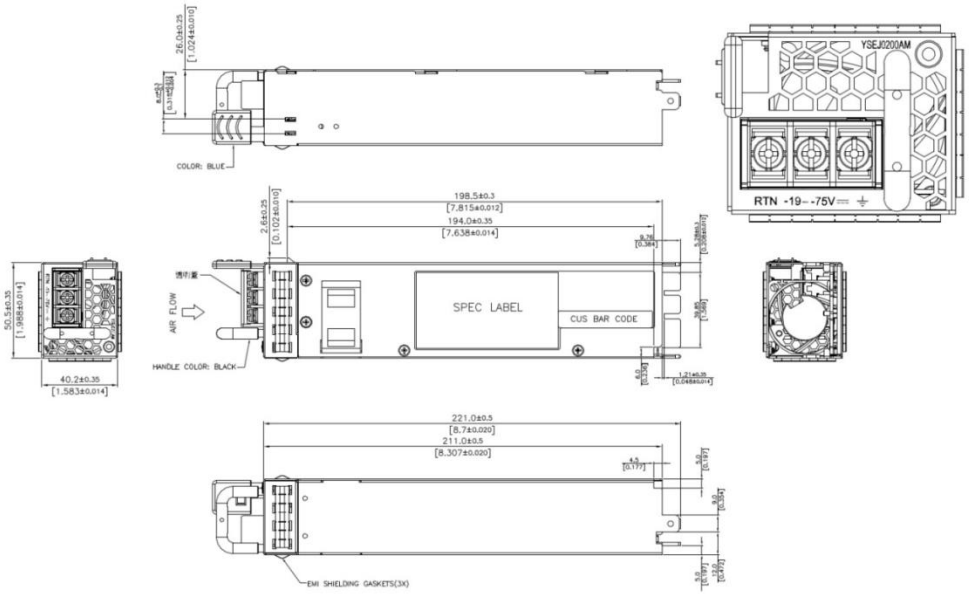


Figure 6-3 200W DC/DC Power Supply Dimension

6.2.2 Electrical Specifications

The detailed electrical specifications of AC/DC PSU are shown as below:

INPUT SPECIFICATIONS	
Input Voltage Range	90 ~ 264 Vac
Input Frequency	47 ~ 63 HZ
Input Current	3A
Inrush Current	60A max.
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12V
Output Current (Amps)	16A(+12V)
Max Power (Watt)	–40°C to 65°C 200W
Output Voltage (Volts)	+5VSB
Output Current (Amps)	3A (+5VSB)
Efficiency	>88% @20% load, >92 @50% load, >88% @100% load
Ripple P-P (mV) (max.)	+12V:120, +5VSB:50
Total Regulation	±5%
GENERAL SPECIFICATIONS	
Hold-up Time (min.)	16mS@-48VDC
Over Voltage Protection	Latch off
Over Current & Short Circuit Protection	Auto Recovery
Over Temperature Protection	Auto Recovery
FAN Failure Protection	Auto Recovery
Hot Swap	Yes, 1+1 redundant
Load Sharing	Yes
Hi-pot	1500VAC
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–40°C to 65°C
Storage Temperature Range	–40°C to +70°C

Humidity, Non-Condensing	0 to 95% RH
EMI	Meets FCC/CISPR 22 Class A(under 10dB) Specification

Table 6-3 AC/DC Power Supply Specification

The detailed electrical specifications of Neg48 DC/DC PSU are shown as below:

INPUT SPECIFICATIONS	
Input Voltage Range	-36 ~ -75VDC
Input Current	8A max
Inrush Current	75A max.
OUTPUT SPECIFICATIONS	
Output Voltage (Volts)	+12V
Output Current (Amps)	16A(+12V)
Max Power (Watt)	–40°C to 65°C 200W
Output Voltage (Volts)	+5VSB
Output Current (Amps)	3A (+5VSB)
Efficiency	>85% @20% load, >87 @50% load, >87% @100% load
Ripple P-P (mV) (max.)	+12V:120, +5VSB:50
Total Regulation	±5%
GENERAL SPECIFICATIONS	
Hold-up Time (min.)	10mS@-48VDC
Over Voltage Protection	Latch off
Over Current & Short Circuit Protection	Auto Recovery
Over Temperature Protection	Auto Recovery
FAN Failure Protection	Auto Recovery
Hot Swap	Yes, 1+1 redundant
Load Sharing	Yes
Hi-pot	2545VDC
ENVIRONMENTAL SPECIFICATIONS	
Operating Temperature Range	–40°C to 65°C
Storage Temperature Range	–40°C to +70°C
Humidity, Non-Condensing	0 to 95% RH
EMI	Meets FCC/CISPR 22 Class A(under 10dB) Specification

Table 6-2 DC/DC Power Supply Specification

6.2.3 PSU LED Status Information

PSU LED behavior is shown as below in various conditions, detailed PSU status is stored in PSU EEPROM and can be accessed by BMC through ipmitool commands:

LED behavior for condition Power supply module1 + Power supply module2 (in normal operation), Power supply module2 LED will be solid GREEN in this case.

Power supply Module1 conditions	Module1 LED	Module2 LED
No power input to this PSU or power input Vin UVP triggered	1Hz Flashing Red	Green
Power input Vin valid, 5V standby Vout valid, P12V Vout is not enabled by system	1Hz Flashing Green	
Power input Vin valid, P12V & P5V_STB Vout valid,	Green	

Power supply is in normal operation condition		
Power supply is shut down due to Vin OVP, Vout OVP/UVP/OCP/SCP, OTP events or fan failure	Red	
Power supply is functional but warning events triggered: Vin UVW/OVW, Vout UVW/OVW/OCW/, OTW	Flashing 1sec Red and 1sec Green	

LED behavior for condition Power supply module1 + Power supply module2 (No power input), Power supply module2 LED will be 1Hz flash RED or off in this case.

Power supply Module1 conditions	**Module1 LED**	**Module2 LED**
No power input to all PSUs (Module1 & Module2)	Off	Off
Power input Vin UVP triggered	1Hz Flashing Red	1Hz Flashing Red
Power input Vin valid, 5V standby Vout valid, P12V Vout is not enabled by system	1Hz Flashing Green	
Power supply is shut down due to Vin OVP, Vout OVP/UVP/OCP/SCP, OTP events or fan failure	Red	
Power supply is functional but warning events triggered: Vin UVW/OVW, Vout UVW/OVW/OCW/, OTW	Flashing 1sec Red and 1sec Green	

Notes:
OVP: Over Voltage Protection
UVP: Under Voltage Protection
OCP: Over Current Protection
OTP: Over Temperature Protection
SCP: Short Circuit Protection
Fan failure: RPM<800 when DC power input is valid for this PSU.
OVW: Over Voltage Warning
UVW: Under Voltage Warning
OCW: Over Voltage Warning
OTW: Over Temperature Warning

Figure 6-4 LED Status Information of PSU

7 Software Support

The S9501 Series supports a base software package composed of the following components:

BIOS
The S9501 Series supports AMI AptioV BIOS with the x86 CPU module

BMC
The S9501 Series supports AMI MegaRAC SP-X BMC firmware for Aspeed AST2600 platform.

ONIE
See http://onie.org/ for the latest supported version

8 Compliance

Environmental	
Operating temperature	-40~65°C
Storage temperature	-40~70°C (–40°F to 158°F)
Operating relative humidity	5%-95% RH (non-condensing)
Storage relative humidity	5%-55% RH (non-condensing)
Dimensions (height x width x depth)	440.0 mm (W) x 302.0 mm (D) x 43.5 mm (H)
Weight	5.9kg

Regulatory Compliances	
Safety	UL 62368-1 IEC/EN 60950-1 IEC/EN 62368-1 BSMI CNS 14336-1
EMC	FCC Part 15, Subpart B, Class A EN55032, Class A EN 300 386 EN 55024 EN 301 489-1 EN 301 489-19 EN 303413 BSMI (CNS 13438), Class A

9 Appendix A – Requirements for IC Approval

Requirements	Details	Link to Section
Contribution License Agreement	OCP CLA, OCPHL Permissive	Section 1
Are all contributors listed in Section 1: License?	Yes	Section 1
Did All the Contributors sign the appropriate license for this spec? Final Spec Agreement/HW License?	Yes	Section 1
Which 3 of the 4 OCP Tenets are supported by this Spec?	Openness Efficiency Impact Scale	UfiSpace IC Presentation (Tenants on slide 12)
Is there a Supplier(s) that is building a product based on this Spec? (Supplier must be an OCP Solution Provider)	Yes	UfiSpace (OCP Solution Providers Directory)
Will Supplier(s) have the product available for GENERAL AVAILABILITY within 120 days?	Yes	Appendix B

10 Appendix B – UfiSpace – OCP Supplier Information

Table of supplier information for the S9501 Series Disaggregated Cell Site Gateway Routers

Supplier Information	
Company	Ufi Space Co. Ltd.
Contact Info	sales@ufispace.com
Product Name	Disaggregated Cell Site Gateway Router
Product SKU#	S9501-28SMT S9501-18SMT
Link to Product Landing Page	S9501-28SMT S9501-18SMT

Summary of supplier requirements

Requirements	Details	Link to Section
Which Product recognition?	OCP Accepted™	Pending Approval
If OCP AcceptedTM, who provided the Design Package?	UfiSpace	Pending Approval
2021 Supplier Requirements for your product(s)		Pending Approval